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10/561,552	03/20/2006	Hidetoshi Nishikawa	19415-005US1 PCT-04R-155/	9795
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EXAMINER				
TAN, VIBOL				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/561,552

Applicant(s)

NISHIKAWA, HIDETOSHI

Examiner

Vibol Tan

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1, 3-8 and 18 is/are allowed.
- 6) ☒ Claim(s) 9 and 11 is/are rejected.
- 7) ☒ Claim(s) 10 and 12-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF-08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claim 9 is rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art in Figs. 11 and 12.

In claim 9, Figs. 11 and 12 of Applicant's admitted prior art teaches, a semiconductor integrated circuit device comprising an output buffer circuit (Fig.11) composed of a logic gate (NO1) that receives data (DATA) and a driver transistor (Tx) that receives, at a control electrode (gate of Tx) thereof, an output from the logic gate (output signal from NO1) and that is driven according to the output from the logic gate, wherein there is provided, within the output buffer circuit, a transistor switch (S1) having a plurality of transistor switches (Tn, Tp in Fig. 12) that have different on-state resistances (on-state resistance for Tn is different from on-state for Tp) and that are connected in parallel (Fig. 12) between the output (output from NO1) of the logic gate and the control electrode of the driver transistor (the gate of Tx), and wherein one of the plurality of transistors is turned on to switch a rate of change (resistance value) of an output of the driver output transistor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior arts.

In claim 11, Figs. 11 and 12 of Applicant's admitted prior art teaches all claimed features the semiconductor integrated circuit device according to claim 9; with the exception of teaching wherein by making MOS transistors constituting each transistor switch have different gate widths and different gate lengths, the transistor switches are made to have different on-state resistances. However, it would have been obvious to one ordinary having the skill in the art at the time the invention was made to make MOS transistors constituting each transistor switch have different gate widths and different gate lengths, the transistor switches are made to have different on-state resistances, since such modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to select different gate widths and gate lengths of

the transistors switches for the prior art circuit in Figs. 11 and 12, as a matter of design choice depends on system involved.

5. Claims 10 and 12-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 1, 3-8 and 18 appear to comprise allowable subject matter.

Response to Arguments

7. Applicant's arguments filed 5/22/2008 have been fully considered but they are not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., if the operating frequency is low, then the selection control signal SELECTION turns on transistor T7a (but not T7b). This results in a higher combined resistance of the circuit to the gate of driver transistor Tx than if the transistor T7b (and not T7a) were turned on. With this higher combined resistance, changes in the gate voltage at driver transistor Tx are gradual. If, on the other hand, the operating frequency is high, then the selection control signal SELECTION turns on transistor T7b (but not T7a). This results in a lower combined resistance of the circuit to the gate of driver transistor Tx than if transistor T7a (but not T7b) were turned on. With this lower combined resistance, changes in the gate voltage at driver transistor Tx are sharp) are not recited in the rejected claim 9. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is

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respectfully submitted that the Applicant's admitted prior art of Figs. 11 and 12, anticipates all claimed features of claim 9; while claim 11 is being obvious over the Applicant's admitted prior art.

The rejection of claims 9 and 11 is maintained.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner
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